Hardware Optimized Beam Steering Electronics for MEOLUT Phased Array Antenna

Priyanka Das*, Yogesh Prasad K R, Ramalaksmi N, Parimal Kumar
ISRO Satellite Centre, Vimanapura, Bangalore: 560017, India
(*Corresponding author: priyadas@isac.gov.in)

Abstract:

A novel hardware-sharing approach is proposed to optimize the design of a beam-forming network for a 13-panel MEOLUT phased array antenna. Band-pass sampling has been employed in digital receiver to allow the switching of common hardware between different panels with sufficient timing margins. Proof-of-concept has been demonstrated by simulations. Experimental results corroborating the simulations have also been presented.

Keywords — Phased array antenna, Beam Steering, Band-pass sampling, digital receiver.

I. INTRODUCTION

MEO Local User Terminal (MEOLUT) is a ground processing station to receive, decode and locate 406 MHz distress beacons globally in near real time for Search And Rescue (SAR) operations . MEOSAR system [1] requires multiple simultaneous time and frequency measurements of distress signal relayed from different satellites to calculate beacon location to the required accuracy. A MEOLUT with the capability of simultaneously tracking multiple satellites with multiple antennas can act as a stand-alone facility for locating the beacon. For such a facility, design of an electronically steerable Phased Array Antenna (PAA), with multiple-beam forming capability is studied as a replacement for multiple reflector-antennas with associated servo mechanisms for mechanical steering. The PAA is required to have a hemispherical coverage and capability to receive LCP/RCP signals simultaneously from at-least ten satellites. A 13-panel PAA configuration, each panel housing 91 microstrip patch antennas, meets this requirement. The 13 panels of PAA can generate an equal number of independent beams to track 13 navigation satellites at any instant.

Following a conventional approach (Fig. 1) requires 13 x 91 Amplifier/Phase-shifter modules and SPDT RF switches in addition to thirteen 91-way power combiners and a PAA controller unit. The large number of antenna elements and the associated hardware involved in the design calls for hardware optimization. In this paper, an optimized design is presented taking into consideration the hardware aspects of PAA and the Digital Receiver processing methodology.

II. CONCEPT OF HARDWARE SHARING

The receiver following the RF front-end, being digital in nature, processes signals that are discrete in time. The interval between two consecutive samples can be effectively utilized to multiplex different panels of PAA to the same set of Amplifier / Phase-shifter modules (Fig. 2).

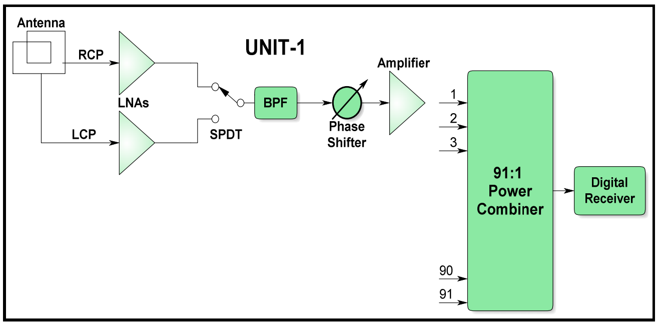

Fig. 1 RF Front end of MEOLUT: Conventional Approach

The number of panels that can be multiplexed depends on the time required for switching between the panels and the time interval between successive samples. Switching time is constrained by the response time of the components used and is fixed for a given design. Hence, it is possible to implement hardware sharing between more number of panels by increasing the sampling time as long as Nyquist criterion [2] is not violated. In this context, Band-Pass Sampling [3], [4] proves to be a better alternative to conventional Low-Pass Sampling [5].

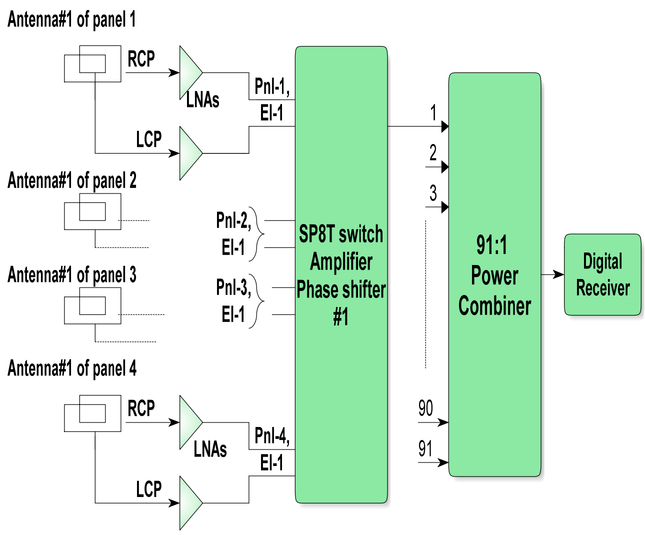

Fig. 2 RF Front end of MEOLUT: Hardware Sharing Approach

III. BAND-PASS SAMPLING

To get optimum performance for a band-limited signal, sampling rate has to be chosen so that the unwanted alias of the signal lies as far as possible from the desired signal. The general condition for optimum separation is [4]:

$$f = n\, f_s \pm ¼\, f_s,\ f_s \geq 2\,BW \qquad (1)$$

where f = centre frequency of the signal being sampled,
f_s = sampling frequency,
BW = Bandwidth,
n = an integer.

For the sake of demonstration it has been assumed that the IF signal obtained after down-conversion is centered at 4 MHz. Bandwidth of 470 KHz, which is double the actual requirement of the downlink signal [1], has been considered for demonstrating the concept. This choice of bandwidth ensures that a lower bandwidth signal poses no difficulties during processing.

From equation (1), it can be seen that a lower value of n results in higher sampling frequency which translates to lesser time margins for switching between the panels. On the other hand, higher value of n allows more number of panels to share a common set of Amplifier / Phase-shifter modules. However, hardware failure will result in non-availability of all the panels involved in sharing. From these considerations, it has been decided to share common hardware between 4 panels.

For the application considered, the IF signal is centered around 4 MHz. The worst-case bandwidth of this BSPK modulated signal is 470 KHz. In our study, f_s is chosen as 0.94 MHz, corresponding to n=4 in equation (1). For a sampling frequency of 0.94 MHz, the interval between successive samples would be 1.063 microseconds. When a common hardware is associated with 4 panels, the time available for each channel would be 265.75 ns. As high-speed RF switches exhibiting switching time of 50 ns (maximum) are readily available, sufficient timing margins exist for switching between the panels.

Fig. 2 illustrates the concept of hardware sharing between four panels. As MEOLUT has to support LCP and RCP polarizations, the antenna elements used in the design are dual polarized. The signals received from the two ports of the antenna are connected to LNAs. The LNA outputs are connected to a common set of Amplifier / Phase-shifter modules through RF switches such that each Amplifier / Phase-shifter module supports one of the four dual-polarized patch antenna elements at any given time. The distribution in the design is such that antenna element # N of 4 different panels are connected to the corresponding common Amplifier / Phase-shifter module # N through an SP8T switch. The 91 outputs of the shared hardware unit are connected to a power combiner and subsequently to a digital receiver.

IV. SIMULATION RESULTS

Digital receiver based on Costas Loop was implemented in MATLAB to demonstrate the concept of band-pass sampling. The block diagram of the demodulator is shown in Fig. 3. The IF and sampling frequencies have been chosen as explained in the earlier section.

Figures 4 to 6 refer to the performance of the receiver when no external noise is added. Fig. 4 shows the control signal of the NCO. Figures 5 and 6 show the modulating data and the recovered demodulated data at one of the arms of the Costas Loop.

Figures 7 to 9 refer to the performance of the receiver when the modulated signal is passed through an AWGN channel. It can be observed from Figs. 8 and 9 that the data can still be demodulated satisfactorily. In the actual scenario, an Integrate and Dump circuitry is introduced after the demodulator. This improves the SNR and hence the BER performance of the receiver. It has been observed that the BER performance obtained by band-pass sampling is comparable to that obtained by normal sampling, under ideal and noise-affected conditions.

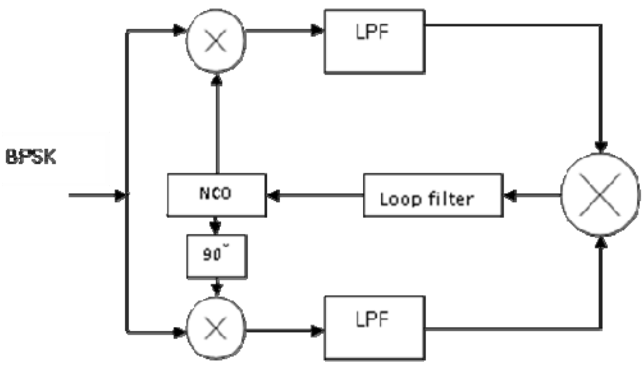

Fig. 3 Costas loop for BPSK Demodulation

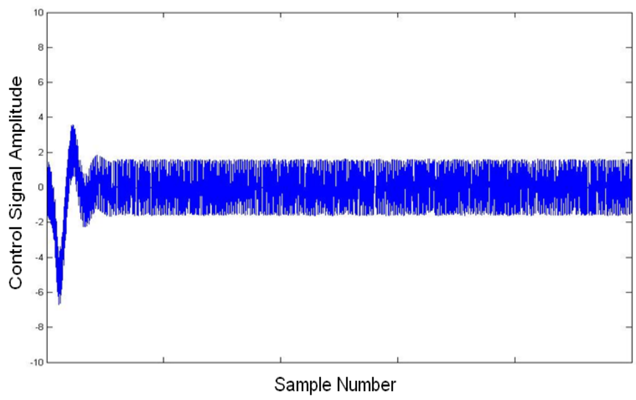

Fig. 4 Control signal to NCO

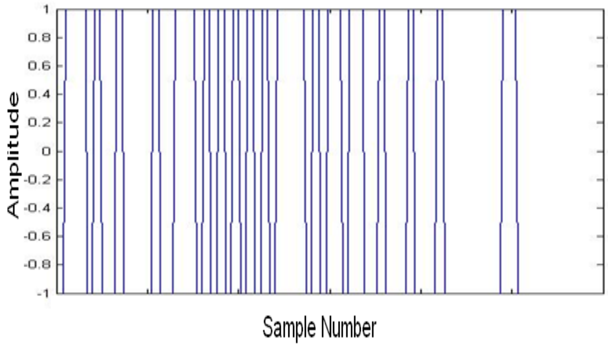

Fig. 5 Modulating Data

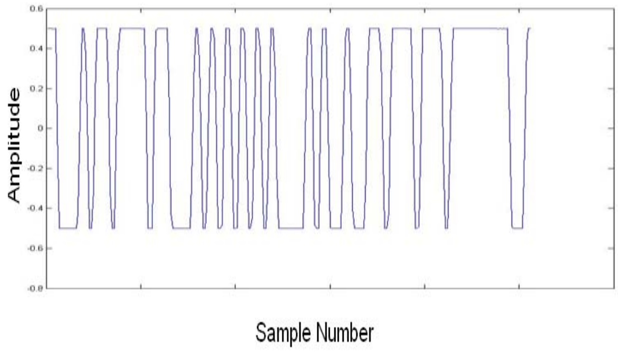

Fig. 6 Demodulated Data

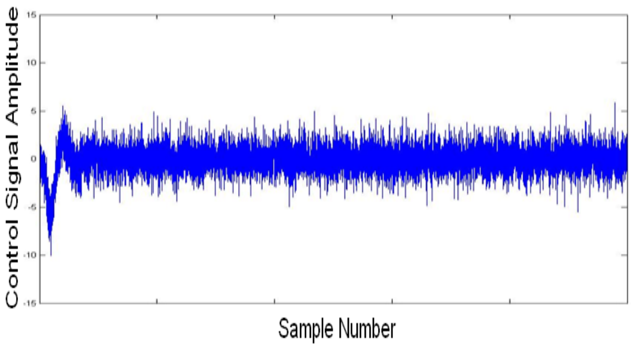

Fig. 7 Control Signal to NCO for a Noisy Signal

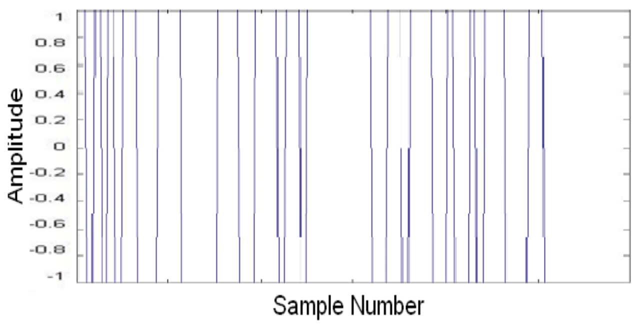

Fig. 8 Modulating Data

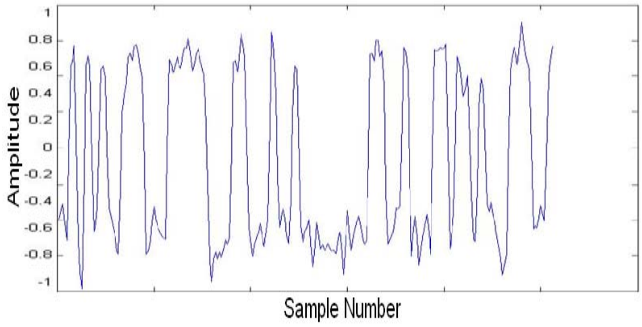

Fig. 9 Demodulated Data in presence of noise

V. IMPLEMENTATION RESULTS

The scheme simulated in MATLAB was implemented practically using Virtex II FPGA. Fig. 10 illustrates the block schematic implemented to demonstrate the use of band-pass sampling for the chosen application. In Fig. 11, the demodulated data obtained using Band-Pass Sampling is compared against the PRBS modulating data. Figs. 12 and 13 show the results obtained using band pass sampling and low pass sampling respectively, for “1010…” data. It may be noted that a BPSK signal centered at 1 MHz and having a bandwidth of 470 KHz was considered for the demonstration. Low Pass Sampling (LPS) was carried out on the BPSK signal at a sampling frequency of 4 MHz. Band pass Sampling (BPS) was carried out at 0.94 MHz. The quality of demodulated data obtained by band-pass sampling is comparable to that obtained by low-pass sampling.

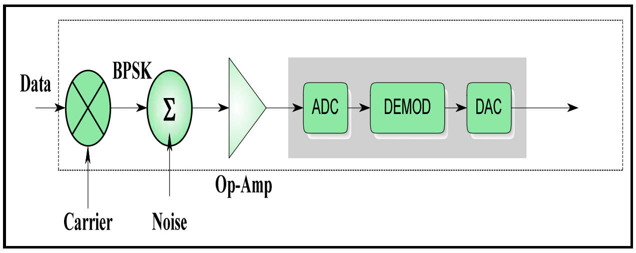

Fig. 10 Set-up for verifying Band-Pass Sampling

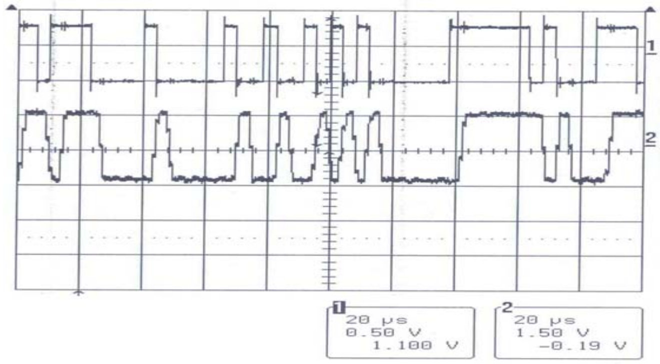

Fig.11 Modulating and demodulated signal for PRBS data with BPS

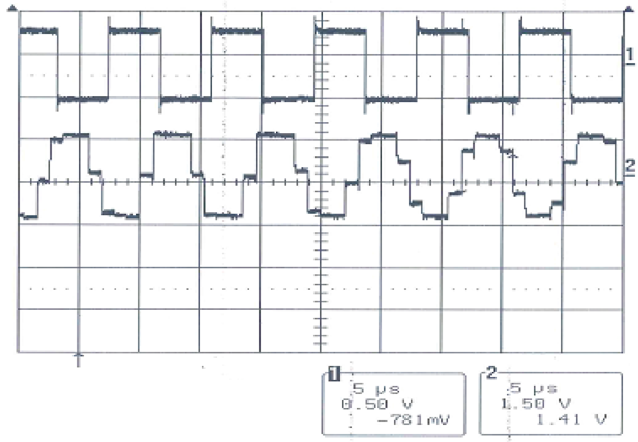

Fig. 12 Modulating and Demodulated Signal for Square data with BPS

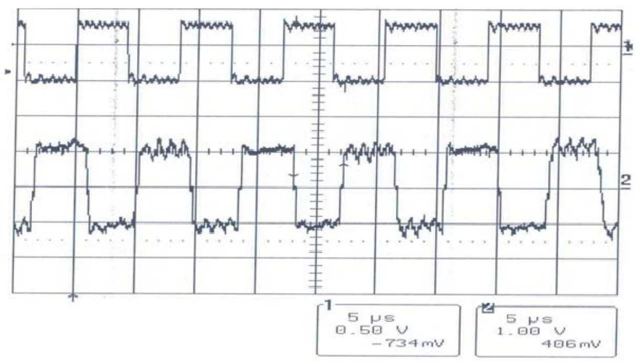

Fig. 13 Modulating and Demodulated Signal for Sqaure data with LPS

VI. COMPARISON OF PROPOSED HARDWARE SHARING APPROACH WITH THE CONVENTIONAL APPROACH

1. Hardware Optimization

For the proposed configuration, where each set of 91 Amplifier and Phase-shifter modules would cater to 4 panels, a total of only 364 Amplifier and Phase-shifter modules as against 1183 would be required to cater to 1183 antenna elements. As amplifier and Phase-shifter modules are quite expensive, reduction in their requirement would considerably lower the total cost. Lesser number of Amplifier and Phase-shifter modules would also mean lesser power dissipation resulting in an easier thermal management.

2. SNR Comparison between LPS and BPS

In a system with a band-pass signal of spectral power density 'S', in-band noise power density 'N_p' and out-of-band noise power density 'N_0', the analog SNR is given by S / N_p. The SNR for the sampled signal becomes degraded by at least the noise aliased from the bands between DC and the passband [6], and is thus given by:

$$SNR_s = S / [N_p + (n\text{-}1)N_0] \qquad (2)$$

where n is the greatest integer contained in (f_u / B), f_u being the highest frequency component of the band-pass signal of bandwidth B.

However, by designing a proper anti-aliasing Band-Pass Filter it is possible to minimize the out-of-band noise N_0. Under such circumstances, the SNR_s shown by (2) approaches S / N_p.

VII. CONCLUSION

In this paper, it has been shown that the hardware sharing scheme can be implemented in conjunction with Band-pass Sampling in digital receiver. MATLAB simulations have been performed to demonstrate the feasibility of Band-Pass Sampling for the band-limited signals that are expected at MEOLUT receivers. The concept has also been implemented successfully using Xilinx Virtex II FPGA board.

It can be concluded that the performance of a Band-Pass Sampling based receiver incorporating an appropriate anti-aliasing band-pass filter would be comparable to that of a Low-Pass Sampling system. Considerable savings in terms of cost and power can be achieved by implementing the hardware sharing approach presented in this paper.

REFERENCE

[1] "COSPAS –SARSAT 406 MHz MEOSAR implementation plan", C/R R.012, Issue –Revision 4, October 2008.

[2] D.A. Linder , "A discussion of sampling theorem, Proc. IRE, vol.47 , 1959.

[3] G. Hill, "The benefits of undersampling,", Electronic Design, July 11, 1994.

[4] "Undersampling applications", Walt Kester, Application Note from Analog Devices.

[5] S. Haykins, "Communication systems", New York: willey,1978.

[6] Rodney G. Vaughan, Neil L. Scott and D. Rod White, "The theory of bandpass sampling", IEEE Transactions on signal Processing, vol.39, No. 9. September 1991.

Priyanka Das received B. Sc. degree in Physics (2006) and B. Tech degree in Radio Physics and Electronics (2009) from Calcutta University, India. She joined ISRO Satellite Centre, Bangalore, in 2009. Her key Interests involve digital communication, digital modulation and Phase array antenna systems and beam steering electronics for LEO missions.

Yogesh Prasad K. R. received his B.E degree in Electronics and Communication Engineering from Andhra University, India in 1998 and M.Tech degree in "Satellite Technology and its Applications" from Indian Institute of Science, Bangalore, India in 2000. He joined ISRO Satellite Center in 2000 and has been working on development of Beam Steering Electronics for Phased Array Antennas and DSP based design implementations.

Ramalakshmi N. received B. Tech degree (1987) from PSG College of Technology, Coimbatore, India and M.S (2013) in Communication Systems from Manipal University, India. Subsequently, she has been working at ISRO. Her research involves antenna systems, RF systems for satellite communication and phased array antenna systems. She has been Deputy Project Director for several satellite missions including Chandrayaan-1 and Mars Orbiter Mission.

Parimal Kumar received his B.E in Electronics and Communication from JNTU, Hyderabad, India in 1983 and M.E in Microwave and Radar from Osmania University, India in 1985. He joined ISRO Satellite Centre in 1986. He was instrumental in development of spacecraft RF systems and ISRO's first Phased Array Antenna for payload data transmission. He is currently working as Project Director for remote sensing mission.